

1     CLAIMS

2     What is Claimed is:

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4           1.     A content addressable memory (CAM) cell  
5     comprising:

6                 a static random access memory (SRAM) cell that  
7                 operates in response to a  $V_{CC}$  supply voltage, the SRAM  
8                 cell storing a data value;

9                 a first set of one or more bit lines coupled to  
10                the SRAM cell, wherein the data value is written to  
11                and read from the SRAM cell on the first set bit  
12                lines, the first set of bit lines having a signal  
13                swing equal to the  $V_{CC}$  supply voltage; and

14                a second set of bit lines coupled to receive a  
15                comparison data value, the second set of bit lines  
16                having a signal swing less than the  $V_{CC}$  supply  
17                voltage.

18  
19           2.     The CAM cell of Claim 1, further comprising a  
20     circuit for comparing the data value with the comparison  
21     data value to determine whether a match exists.

22  
23           3.     The CAM cell of Claim 2, wherein the circuit  
24     comprises:

25                 a first transistor having a gate coupled to  
26                 receive a signal representative of the data value;  
27                 and

28                 a second transistor having a gate coupled to  
29                 receive a signal representative of the inverse of the  
30                 data value.

1           4.    The CAM cell of Claim 3, wherein the second set  
2 of bit lines comprises:

3               a first bit line coupled to a source region of  
4 the first transistor; and

5               a second bit line coupled to a source region of  
6 the second transistor.

7  
8 *7* 5.    The CAM cell of Claim 4, wherein a drain region  
9 of the first transistor is coupled to a drain region of  
10 the first transistor at a first node.  
11

12           6.    The CAM cell of Claim 5, further comprising a  
13 diode element coupled to the first node.  
14

15           7.    The CAM cell of Claim 6, further comprising a  
16 local mask transistor coupled in series with the diode  
17 element.  
18

19           8.    The CAM cell of Claim 6, wherein the diode  
20 element comprises a diode-connected transistor.  
21

22           9.    The CAM cell of Claim 6, wherein the diode  
23 element comprises a P-N junction.  
24

25           10.   The CAM cell of Claim 6, further comprising a  
26 match line coupled to the diode element, wherein the diode  
27 element is forward biased from the match line to the first  
28 node.  
29

30           11.   The CAM cell of Claim 10, wherein the match line  
31 has a signal swing equal to a transistor threshold  
32 voltage.

12. The CAM cell of Claim 10, further comprising a sensor circuit coupled to the match line, the sensor circuit pre-charging the match line to a voltage less than the  $V_{CC}$  supply voltage.

13. The CAM cell of Claim 12, wherein the sensor circuit comprises a logic gate for providing an output signal that indicates whether a match or a no-match condition exists, the output signal having a signal swing equal to the  $V_{CC}$  supply voltage.

14. The CAM cell of Claim 1, further comprising a bit line control circuit for biasing the second set of bit lines.

15. The CAM cell of Claim 14, wherein the bit line control circuit comprises a first transistor for connecting the second set of bit lines during a pre-charge operation.

16. The CAM cell of Claim 14, wherein the bit line control circuit comprises one or more transistors for connecting the second set of bit lines to a voltage supply line during a global masking operation, the voltage supply line having a voltage less than the  $V_{CC}$  supply voltage.

17. The CAM cell of Claim 14, wherein the bit line control circuit comprises a plurality of transistors for selectively coupling the second set of bit lines to a voltage supply line and a ground supply line, whereby the second set of bit lines receive voltages representative of

1 the comparison data value from the voltage supply line and  
2 the ground supply line, the voltage supply line having a  
3 voltage less than the  $V_{CC}$  supply voltage.

4  
5 18. The CAM cell of Claim 17, wherein the voltage  
6 supply line has a voltage of two times a transistor  
7 threshold voltage.

8  
9 19. The CAM cell of Claim 14, wherein the bit line  
10 control circuit is powered by a supply voltage less than  
11 the  $V_{CC}$  supply voltage.

12  
13 20. A content addressable memory (CAM) cell having a  
14 match line that carries a signal to indicate whether a  
15 match or a no-match condition exists within the CAM cell,  
16 *wherein the difference between a voltage on the match line during the match condition*  
17 ~~the match line having a signal swing equal to one~~ *and a voltage on the*  
18 transistor threshold voltage. *the match line during the no-match condition is*

19  
20 21. A method of operating a content addressable  
21 memory (CAM) cell that includes a static random access  
22 (SRAM) cell, the method comprising the steps of:  
23 operating the SRAM cell in response to a  $V_{CC}$   
24 supply voltage, the SRAM cell storing a data value;  
25 writing a data value to the SRAM cell on a first  
26 set of one or more bit lines, the first set of bit  
27 lines having a signal swing equal to the  $V_{CC}$  supply  
28 voltage;  
29 reading data values from the SRAM cell on the  
30 first set of bit lines;  
31 controlling the signal swing on the first set of  
bit lines to be equal to the  $V_{CC}$  supply voltage;

Concluded  
but 82

1 providing comparison data values to the CAM cell  
2 on a second set of bit lines; and

3 controlling the signal swing on the second set  
4 of bit lines to be less than the  $V_{CC}$  supply voltage.  
5

6 22. The method of Claim 21, further comprising the  
7 step of comparing the data value stored in the CAM cell  
8 with the comparison data value to determine whether a  
9 match condition or a no-match condition exists.  
10

11 23. The method of Claim 22, further comprising the  
12 step of indicating a match condition and a no-match  
13 condition by providing a signal having a signal swing  
14 equal to one transistor threshold voltage.  
15

16 24. The method of Claim 22, wherein the step of  
17 comparing comprises the step of coupling one of the bit  
18 lines in the second set of bit lines to a match line in  
19 response to the data value stored in the CAM cell.  
20

21 25. The method of Claim 24, further comprising the  
22 step of pre-charging the match line to a voltage less than  
23 the  $V_{CC}$  supply voltage.  
24

25 26. The method of Claim 25, further comprising the  
26 step of discharging the match line when a no-match  
27 condition exists.  
28

29 27. The method of Claim 23, further comprising the  
30 step of converting the signal having the signal swing of  
31 one transistor threshold voltage to a signal having a  
32 signal swing equal to the  $V_{CC}$  supply voltage.

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1  
2 28. The method of Claim 21, further comprising the  
3 step of equalizing the second set of bit lines prior to  
4 providing the comparison data values to the CAM cell on  
5 the second set of bit lines.

6  
7 29. The method of Claim 21, further comprising the  
8 step of connecting the second set of bit lines to a  
9 voltage supply line during a global masking operation, the  
10 voltage supply line having a voltage less than the  $V_{CC}$   
11 supply voltage.

12  
13 30. The method of Claim 21, further comprising the  
14 step of selectively coupling the second set of bit lines  
15 to a voltage supply line and a ground supply line, whereby  
16 the second set of bit lines receive voltages  
17 representative of the comparison data value from the  
18 voltage supply line and the ground supply line, the  
19 voltage supply line having a voltage less than the  $V_{CC}$   
20 supply voltage.

21  
22 31. The method of Claim 30, wherein the voltage  
23 supply line has a voltage of two times a transistor  
24 threshold voltage.

25  
26 32. The method of Claim 21, further comprising the  
27 step of biasing the second set of bit lines with a supply  
28 voltage less than the  $V_{CC}$  supply voltage.

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